IN THE CLAIMS:

Please amend the claims as follows. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor,

wherein a base of the double poly bipolar transistor contains a first dopant having a first dopant concentration and a gate of the double poly metal oxide semiconductor transistor ~~contain substantially identical dopant concentrations~~ contains said first dopant having said first dopant concentration;

wherein an emitter of the double poly bipolar transistor contains a second dopant having a second dopant concentration and a source/drain of the double poly metal oxide semiconductor transistor contains said second dopant having said second dopant concentration;

wherein said semiconductor apparatus further comprises a first polysilicon layer and a second silicon layer that is separate from the first polysilicon layer.

2. (Currently Amended) The semiconductor apparatus as set forth in Claim 1 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor comprise a substrate and a first layer of polysilicon (Poly1) material wherein:

said first layer of polysilicon (Poly1) material in said at least one double poly bipolar transistor is doped with impurity ions of said first dopant to form an extrinsic base; and

said first layer of polysilicon (Poly1) material in said at least one double poly MOS transistor is doped with impurity ions of said first dopant to form [[an]] a MOS transistor gate.

3. (Original) The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

4. (Original) The semiconductor apparatus as set forth in Claim 2 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

5.-6. (Cancelled)

7. (Currently Amended) The semiconductor apparatus as set forth in Claim 2 wherein:

said substrate is implanted with impurity ions of a third dopant to form an intrinsic base in said at least one double poly bipolar transistor; and

said substrate is simultaneously implanted with impurity ions of said third dopant to form a lightly doped drain in said at least one double poly MOS transistor.

8. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said lightly doped drain in said at least one double poly MOS transistor is self aligned.

9. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

10. (Original) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

11.-12. (Cancelled)

13. (Currently Amended) The semiconductor apparatus as set forth in Claim 7 wherein said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor further comprise a second layer of polysilicon (Poly2) material wherein:

said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is doped with impurity ions of said second dopant to form an emitter; and

said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is simultaneously doped with impurity ions of said second dopant to form [[an]] a MOS source/drain.

14. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said emitter in said at least one double poly bipolar transistor is self aligned to an extrinsic base of said at least one double poly bipolar transistor.

15. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said at least one double poly MOS transistor is self aligned to a gate of said at least one double poly MOS transistor.

16. (Currently Amended) The semiconductor apparatus as set forth in Claim 13 wherein said second layer of polysilicon (Poly2) material in said at least one double poly bipolar transistor is simultaneously doped with impurity ions of said second dopant to form a deep collector.

17. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said MOS source/drain in said second layer of polysilicon (Poly2) material in said at least one double poly MOS transistor is etched to separate said MOS source/drain into a source and a drain.

18.-19. (Cancelled)

20. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor.

21. (Original) The semiconductor apparatus as set forth in Claim 13 wherein said at least one double poly bipolar transistor is a PNP transistor and wherein said at least one double poly MOS transistor is an NMOS transistor.

22.-42. (Cancelled)

43. (New) A semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor;

wherein a base of the double poly bipolar transistor contains a first dopant having a first dopant concentration and a gate of the double poly MOS transistor contains said first dopant having said first dopant concentration; and

wherein an emitter of the double poly bipolar transistor contains a second dopant having a second dopant concentration and a source/drain of the double poly MOS transistor contains said second dopant having said second dopant concentration.

44. (New) The semiconductor apparatus as set forth in Claim 43 wherein said at least one double poly bipolar transistor and said at least one double poly MOS transistor comprise a substrate and a first layer of polysilicon material, wherein:

said first layer of polysilicon material in said at least one double poly bipolar transistor is doped with impurity ions of said first dopant to form an extrinsic base; and

said first layer of polysilicon material in said at least one double poly MOS transistor is doped with impurity ions of said first dopant to form a MOS transistor gate.

45. (New) The semiconductor apparatus as set forth in Claim 44 wherein said at least one double poly bipolar transistor and said at least one double poly MOS transistor further comprise a second layer of polysilicon material, wherein:

said second layer of polysilicon material in said at least one double poly bipolar transistor is doped with impurity ions of said second dopant to form an emitter; and

said second layer of polysilicon material in said at least one double poly MOS transistor is simultaneously doped with impurity ions of said second dopant to form a MOS source/drain.

46. (New) The semiconductor apparatus as set forth in Claim 45 wherein:

said substrate is implanted with impurity ions of a third dopant to form an intrinsic base in said at least one double poly bipolar transistor; and

said substrate is simultaneously implanted with impurity ions of said third dopant to form a lightly doped drain in said at least one double poly MOS transistor.

47. (New) The semiconductor apparatus as set forth in Claim 45 wherein said second layer of polysilicon material in said at least one double poly bipolar transistor is simultaneously doped with impurity ions of said second dopant to form a deep collector.